FEB 0 7 2005

INFORMATION DISCLOSURE STATEMENT

Applicants

Jayesh R. Bhakta et al.

App. No

10/765,488

Filed

January 27, 2004

For

ARRANGEMENT OF INTEGRATED

CIRCUITS IN A MEMORY MODULE

Examiner

Ly D. Pham

Art Unit

2818

Alexandria, VA 22313-1450, on 2/4/05

(Date)

CERTIFICATE OF MAILING

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Dear Sir:

Enclosed for filing in the above-identified application is an Information Disclosure Statement by Applicant (PTO/SB/08 equivalent) listing two (2) references to be considered by the Examiner.

This Information Disclosure Statement is being filed before the mailing date of a final action and before the mailing of a Notice of Allowance. This Statement is accompanied by the fees set forth in 37 C.F.R. § 1.17(p). The Commissioner is hereby authorized to charge any additional fees which may be required or to credit any overpayment to Account No. 11-1410.

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Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated:

2/4/05

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INFORMATION DISCLÖSURE
STATEMENT BY APPLICANT

Application No. 10/765,488

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First Named Inventor Jayesh R. Bhakta

Art Unit 2818

Examiner Ly D. Pham

NETL.001DV3

FEB 0 7 2005 (Multiple sheets used when necessary)

SHEET 1 OF 1

TRADEMARY		U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number	Publication Date	Name of Patentee or Applicant	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear		
		5,606,717	02/25/1997	Farmwald et al.			
		6,617,695 B1	09/09/2003	Kasatani			
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Attorney Docket No.

	FOREIGN PATENT DOCUMENTS									
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